Application N .: 09/801,350 **Docket N .: JCLA6643**

REMARKS

I. Present Status of the Application

The Office Action rejected claims 1, 3-4 and 13-14 under 35 U.S.C. § 102(b) as being anticipated by Yu (US 5,869,873). The Office Action also rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Ker et al. (US 5,754,380).

No amendments are made to the application. Claims 1-4, 13 and 14 remain pending in the present application. Applicants believe that this reply does not introduce new matter. Reconsideration of those claims is respectfully requested.

II. Response to Rejections

A. Rejections under 35 U.S.C. § 102(b) over Yu

The Office Action, at pages 2-3, rejected claims 1, 3-4 and 13-14 under 35 U.S.C. § 102(b) as being anticipated by Yu. Applicants respectfully traverse the rejection for at least the reasons set forth below.

Claim 1 of Applicants' invention provides an ESD protection circuit wherein an anti-latch-up signal is sent from an anti-latch-up circuit to a SCR circuit. The signal is issued under normal operation condition to prevent latch-up of the SCR circuit from occurring.

However, Yu does not teach the foregoing feature but something rather different. In Response to Arguments, Examiner asserts that "Yu teaches that the EPROM transistor triggers

the SCR circuit . . . by applying voltage to the SCR circuit," and that "Yu teaches an anti-latch-up circuit providing a voltage to the third terminal of the SCR circuit, as claimed" (Office Action, page 6, items 5 and 6). Applicants respectfully traverse Examiner's assertion. Even if as Examiner stated that the EPROM "triggers" the SCR circuit, Applicants respectfully point out that Examiner incorrectly stated "[t]riggering is done by applying voltage to the SCR circuit." Instead, the triggering occurs only when the EPROM first enters breakdown upon ESD stress occurs (column 5, lines 36-38 and 48; column 2, line 66 through column 3, line 5). EPROM triggers to conduct a discharge current and thus bypass ESD stress (column 3, lines 35-37). The term "trigger" in Yu's disclosure should be interpreted in light of the supporting disclosure. Hence, Yu does not teach an anti-latch-up circuit providing a voltage to the third terminal of the SCR circuit as recited in claim 1 of the present application.

Examiner also states in Response to Arguments that it is unclear as to what is meant by the phrase of "the anti-latch-up circuit ..... prevents the SCR circuit when no ESD occurs" (Office Action, page 6, item 5). Please be noted that the phrase refers the anti-latch-up circuit issues the signal under normal condition even when no ESD occurs (rather than only when ESD stress occurs), which prevents the latch-up of the SCR circuit from occurring. Yu does not teach the foregoing feature since Yu's EPROM transistor triggers the SCR circuit only when ESD stress occurs.

Further, Yu discloses that the EPROM transistor during the normal operation is in an off state, i.e., there is no signal transmission between the RC circuit and the SCR circuit. As Examiner stated that the terms in a claim are given interpretation in light of the supporting

disclosure. However, based on the specification of the present invention, the term of "coupled" in claim 3 refers that there is signal transmission between the RC circuit and the SCR circuit. Because there is no signal transmission between the RC circuit and the SCR circuit during the normal operation, it should be reasonable to state that Yu's EPROM device does not couple the RC circuit to the SCR circuit.

Besides, according to Yu's disclosure (column 5, lines 24-40), a RC circuit (Fig. 6) is used "to program the EPROM" to raise "the threshold voltage of the EPROM" during an ESD event. That is, the signal from the RC will be coupled to "the control gate of the EPROM," instead of the third terminal of SCR as recited in claim 1 of the present application.

Therefore, the claim 1 is not anticipated by Yu since Yu does not disclose each and every element of the claim. Claim 3 is not anticipated by Yu even if the term of "couple" is construed as Examiner asserts, since the parent independent claim 1 is patentable at least for the foregoing reasons. Similarly, claims 4 and 13-14 are not anticipated by Yu due to their dependency upon the claim 1.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that the grounds of rejection have been addressed and the rejection overcomes. Reconsideration and withdrawal of the rejection are respectfully requested.

B. Rejections under 35 U.S.C. § 103(a) over Yu in view of Ker et al.

The Office Action, at pages 4-5, rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Ker et at. The Examiner asserts that it would have been obvious

to a person of ordinary skill in the art at the time the invention was made to incorporate Ker et al.'s teaching into Yu's device in order to provide better protection for the device against ESD event. Applicants respectfully traverse the rejection.

As discussed in the foregoing section, the underlying working principle as claimed in claim 1, which is the parent claim of claim 2 at issue, is significantly distinguishable from that taught by Yu. For example, Yu teaches that "[w]hen ESD stress occurs to the pad, the EPROM enters breakdown and triggers the SCR to operate in the snapback region for by passing the ESD stress in order to prevent the internal circuit form ESD damage" (column 5, lines 47-50). Clearly, Yu's EPROM does not function as the anti-latch-up circuit of Applicants' invention as recited in claim 2 or claim 1.

Yu does not suggest or motivate one of ordinary skill in the art at the time the invention was made to use a pair of diotes, as disclosed in Ker et al., to make an improvement as claimed in the present invention. Due to significant difference in underlying working principals between Applicants' claimed invention and Yu's disclosure as discussed in the foregoing, even if an analog were made to combine the techniques in the two references of Yu and Ker et al., the resulting technique would have been still significantly different from that of claim 2.

For at least the foregoing reasons, it is clear that the ESD protection circuit recited in claim 2 is not within the scope of and thus not simple analogs of those disclosed by Yu. As considered as a whole, even if the Ker et al. disclose the use of a pair of diotes, it seems clear that one of ordinary skills in the art is not suggested or motivated to combine the technique of Ker et

al. with the device disclosed in Yu to provide improvements for creating the ESD protection circuit recited in claim 2.

Therefore, claim 2 is not obvious over Yu either alone or in combination with Ker et al. Accordingly, Applicants respectfully submit that the grounds of rejection have been addressed and the rejection overcome. Reconsideration and withdrawal of the rejection are respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-4, 13 and 14 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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